TH

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/764,905 | 01/26/2004 | Sang Hun Oh | PIA31205/ANS/US | 2660 |

36872 7590 06/14/2007

THE LAW OFFICES OF ANDREW D. FORTNEY, PH.D., P.C.
401 W FALLBROOK AVE STE 204
FRESNO, CA 93711-5835

| EXAMINER | |
|---|---|
| SULLIVAN, CALEEN O | |
| **ART UNIT** | **PAPER NUMBER** |
| 1756 | |
| **MAIL DATE** | **DELIVERY MODE** |
| 06/14/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/764,905 | OH, SANG HUN | |
| | Examiner | Art Unit | |
| | Caleen O. Sullivan | 1756 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-5,7 and 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/08/07; 04/09/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. Applicant's amendment to claim 1 as well as the arguments presented has overcome the rejection of claims 1-6 under 35 USC 112 first paragraph as well as the rejection of claims 1-6 under 35 USC 112 second paragraph. Therefore, Examiner has withdrawn those rejections.

2. Applicant's amendments to claims 1-5 and the addition of claim 7 have not overcome the rejection under 35 USC 103(a) presented in the last Office Action. Therefore, Examiner restates the grounds of rejection presented in the last Office Action in response to the amendments and the addition of claim 7.

3. In response to Applicant's addition of claim 8, Examiner presents a new ground of rejection below.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. 6. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa ('704) and Wang ('840) in view of Grill ('725) and Gardner ('379).

Furukawa ('704) teaches a process to fabricate a short channel field effect transistor with a highly conductive gate. In this process a first insulating layer is deposited on a substrate over which a conductive forming layer, then a conductive layer, then another insulating layer and lastly a photoresist layer are deposited. (See, col.7, 50-67). The resist layer is exposed to actinic light and developed down to the second insulating layer. (See, col.8, 5-8). This disclosure in Furukawa ('704) meets the limitations of claim 1 where a structure, comprised of a lower insulating layer, a lower metal line and then an upper insulating layer is covered with a layer of photoresist that is patterned and then used a mask.

The portion of the second insulation layer that is beneath the opening in the photoresist is removed down to the second conductive layer by etching. (See, col.8, 9-14). This process step disclosed in Furukawa ('704) teaches the limitation of claim 1 where the upper insulating layer is etched until at least a portion of the lower metal line is exposed. After the photoresist layer is stripped (See, col.8, 14) as recited in claim 3, the trench created in the upper insulating layer is filled with a third insulating material, and Furukawa ('704) teaches silicon nitride is one such suitable insulating material. (See, col.8, 14-18). This step in the process meets the limitation of claim 1 where the etched portion of the upper insulating layer is filled with a nitride film.

Then the second insulating layer is removed by etching (See, col.8, 24-25) as recited in claim 4, followed by a step of etching the conductive layer using the insulating material that filled the trench as mask. (See, col. 8, 24-29 and Fig.7). This step in the process meets the limitation of claim 1 where the lower metal line is etched until the lower insulating layer is exposed. Lastly, the first

insulating layer is etched using the nitride insulation layer the conductive layer and the conductive forming layer as a mask. (See, col.8, 24-29).

Furukawa ('704) fails to teach a process where a second photoresist layer is deposited, patterned, used as a mask and removed. Furukawa ('704) also fails to teach a step where an IMD layer is deposited forming an air gap within the IMD layer, that is later planarized, after which a nitride layer is etched and the trench formed is filled with a conductive material. Furukawa ('704) also fails to disclose a process step where an upper metal line is deposited over the conductive material by an Al/Cu damascene process. However, Wang ('840) discloses a process, which teaches the steps of patterning a second photoresist layer, which is then used as a mask before being removed. Wang ('840) also teaches a step where a nitride layer is etched and the trench formed is filled with a conductive material over which an upper metal line is formed.

Wang ('840) teaches a process for forming a dual damascene structure. The process uses a structure consisting of a substrate on which a patterned metal layer is formed over which a dielectric layer is deposited. The structure also includes a stop layer formed over the first dielectric layer and then another dielectric layer is formed over the stop layer. (See, col. 2, 49-53 and Fig.1 and 2A). A first photoresist layer is formed on the upper dielectric layer and is used to define the first dielectric layer the stop layer and the second dielectric layer, and the portions of the three layers not covered by the photoresist layer are removed to form a via opening. (See, col. 2, 60-67).

Wang ('840) then discloses another dielectric layer is formed over the structure that fills a portion of the via formed in the upper dielectric layer. (See col. 3, 6-22). Then a second layer of photoresist is formed on the dielectric layer, which is used as an etch mask to pattern the various dielectric layers (See, col.3, 23-34), and the dielectric layer and material deposited in the via are completely removed to expose the metal layer. (See, col.3, 31-34). This disclosure teaches the

limitations in claim 1 where a second photoresist layer is patterned and used as an etch mask as well as the limitation of claim 4 where the upper insulating layer is removed. After the second patterning and etching steps the second photoresist layer is removed (See, col. 3, 37-38) as recited in claim 5.

Wang ('840) also discloses another step in the process where a conductive material, such as a metal, is formed over the dielectric layer, and fills the via and trench formed. (See, col. 3, 39-54). The conductive material is removed from the dielectric layer by chemical mechanical polishing exposing the dielectric layer, and after filling the via opening with the conductive material a via plug is formed. (See col. 3, 39-54). Then, an upper level conductive liner is formed by filling the trench with conductive material. (See, col.3, 39-54 and Fig. G). These steps disclosed in Wang ('840) meet the limitations of claim 1 where the hole formed in a dielectric layer is filled with conductive material and an upper metal line is deposited over the conductive material.

However, Wang ('840) also fails to teach the upper metal line is formed by an Al/Cu damascene process. Deposition of an upper metal line by such a method is disclosed in Grill ('725). Grill ('725) teaches a method of forming a multilevel interconnect structure that contains air gaps. Grill ('725) discloses the steps followed in a typical damascene process (See, col. 1, 56-67), and Grill ('725) teaches the conductive wiring formed during this process can include metals or alloys such as an Al-Cu alloy. (See, col.5, 37-40). The teachings of Grill ('725) meet the limitation of claim 2, where the deposition of the upper metal line comprises an Al/Cu damascene process.

Wang ('840) also fails to teach the limitations of claim 1 where an IMD layer is deposited on the structure, an air-gap is formed within the IMD layer and the IMD layer is planarized. A method teaching process steps such as these is disclosed in Gardner ('379).

Gardner ('379) teaches a method of forming an air gap spacer for high performance MOSFETS, including planarizing the interlevel dielectric. The process uses a structure comprised of

a substrate over which a dielectric layer, a polysilicon layer that is rendered conductive by doping, and a masking layer are deposited. (See, Fig.2). Portions of the polysilicon layer and masking layer are removed to form gate conductors. (See, Fig.5-6 and col.5, 32-39). An inter level dielectric is CVD deposited over the surface of a semiconductor topography between the laterally adjacent gate conductors. (See, col. 6, 66-col.7, 13). The masking structures above the gate conductors on the semiconductor prevent the dielectric material deposited from accumulating on the sidewall surfaces of the gate conductors and air gaps are formed laterally adjacent to the gate conductors. (See, col.7, 1-13). The interlevel dielectric is removed to a level that is substantially coplanar with the upper surface of the masking structure by using a chemical mechanical polishing. (See, col.7, 11-13 and Fig.12). These process steps teach the limitations of claim 1, where an IMD layer is deposited, an air gap is formed within the IMD layer, the IMD layer is planarized to expose the nitride film, as well as the limitation of claim 7.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to combine the teachings of Furukawa ('704) and Wang ('840) with the teachings of Grill ('725) and Gardner ('379) in order to form an air gap within a dielectric layer between conductive or metal layers, which Grill ('725) teaches can be formed by a damascene process using an Al-Cu alloy, because Gardner ('379) teaches the inclusion of air gaps between the conductive layers prevents unwanted capacitive coupling because the dielectric constant of the dielectric material between the multiple conductive layers has been lowered by including the air gaps.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa ('704) and Wang ('840) in view of Grill ('725) and Gardner ('379) as applied to claims 1-5 and 7 in paragraph 6 above, and further in view of Yasushi. Furukawa ('704) and Wang ('840) in view of Grill ('725) and

Gardner ('379) fail to disclose a process step where the nitride film is removed by wet etching. However, Yasushi discloses such a process step.

Yasushi discloses a method of manufacturing a semiconductor device. Yasushi discloses that a passivation film (4) is laid on a substrate on which a gate (2) and a source-drain (3) electrode are formed. (See, abstract). Yasushi discloses that, a resist (5) layer is applied over the electrodes, and is removed above the gate (2) electrode. (See, abstract). Then Yasushi discloses a plasma silicon nitride (6) film is grown on the whole face and the resist (4) is removed, leaving the nitride film only at the part above the gate (2) electrode. (See, abstract). Yasushi discloses that next wiring (7) to be connected to the source-drain (3) electrode is formed on the nitride film, which is then removed by wet etching. (See, abstract). This disclosure meets the limitation of claim 8.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the combination of Furukawa ('704), Wang ('840), Grill ('725) and Gardner ('379) with the teachings of Yasushi, because Yasushi teaches that one can remove a nitride layer, formed during a process to fabricate a semiconductor device, using a wet etching process step.

***Response to Arguments***

9. Applicant's arguments filed 04/09/2007 have been fully considered but they are not persuasive.

10. Applicant first argues that Furukawa ('704) fails to discloses stacking a lower insulating layer, a lower metal line and an upper insulating layer; however, in Fig. 5, one finds such a structure and the process of forming the structure is disclosed in col. 7, lines 50-67. The structure consists of a substrate (1) on which an insulating layer (3), a conductive forming layer (4), a conductive layer (27) and then an insulating layer (5) are formed. Overlying the aforementioned layers is a resist (6) layer. Therefore, Furukawa ('704) does disclose the structure formed in claim 1 of the present application.

Applicant also argues Furukawa ('704) fails to disclose planarizing an IMD layer and then removing the nitride layer to form a contact hole in the IMD layer to expose the upper surface of the lower metal line. Applicant further argues that Furukawa ('704) is silent as to voids or air/gaps in a dielectric layer. However, Examiner did not rely upon Furukawa ('704) in the previous rejection or in this rejection as teaching such limitations.

12. Next, Applicant argues that Wang ('840) fails to disclose planarizing an IMD layer to expose nitride film and then removing the nitride film to form a contact hole in the IMD layer to expose upper surface of the lower metal line as well as filling the contact hole with conductive material. Moreover, Applicant argues that Wang ('840) fails to disclose filling an etched portion of the upper insulating layer with a nitride film layer. However, Examiner did not rely upon Wang ('840) in the previous rejection or in the present rejection as teaching such limitations.

13. Then Applicant argues that Grill ('725) fails to disclose filling an etched portion of an upper insulating layer with a nitride film, planarizing a IMD layer to expose the nitride film and removing the nitride film to form a contact hole in the IMD layer and expose upper surface of the lower metal line. Furthermore, Applicant argues that Grill ('725) fails to disclose deposing an IMD layer on lower metal line pattern and a nitride film layer thereby forming an air gap in the IMD layer between metal lines in the lower metal pattern. However, Examiner did not rely upon Grill ('725) in the previous rejection or in the present rejection as teaching such limitations.

14. Lastly, Applicant argues that Gardner ('379) also fails cure the deficiencies of Furukawa ('704). Applicant states that Gardner ('379) discloses masking structures that may be composed of nitride or oxide or silicon oxy-nitride or a metal. Applicant argues that based on this disclosure Gardner ('379) can only disclose filling an etched portion of the upper insulating layer with a nitride film or Gardner ('379) can only disclose stacking a lower insulating layer, a lower metal line and then

an upper insulating layer. However, Examiner did not rely upon Gardner ('379) in the previous rejection or in the present rejection as teaching such limitations. Furthermore, Applicant's arguments regarding what Gardner ('379) can or cannot disclose, unfairly limits the breadth of Gardner ('379), because a reference is applicable for what it teaches explicitly and implicitly.

Applicant also states that Gardner ('379) is silent regarding the removal of the nitride masking structures, which prevent the dielectric material deposited on the structure from forming on the sidewalls of the gate conductors, whereby air gaps are formed laterally adjacent to the gate conductors. (See, col.7, 1-13). Applicant argues that Gardner's ('379) failure to disclose such a step means Gardner ('379) fails to disclose a step of removing the nitride film to form a contact hole in the IMD layer that exposes the upper surface of the lower metal line. However, Examiner did not rely upon Gardner ('379) in the previous rejection or in the present rejection as teaching such limitations.

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

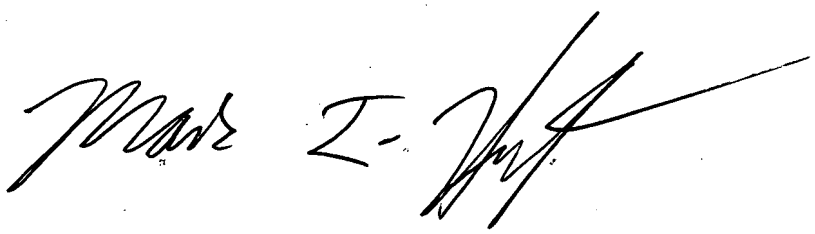
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Caleen O. Sullivan whose telephone number is 571-272-6569. The examiner can normally be reached Monday-Friday, 8:30am-5:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff can be reached on 571-272-1385. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/COS/, 05/30/2007



MARK F. HUFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700